In the Claims:

Claim 1 (currently amended): A method comprising steps of:

forming a layer over a transistor gate region and a field oxide region, said transistor gate region being situated over a well and said field oxide region not being situated over said well, wherein said field oxide region and said well are situated in a substrate;

forming a doping barrier above said layer over said field oxide region;

doping said layer over said transistor gate region with a first dose of a first dopant, wherein said dose of said first dopant is a dosage greater than required to result in said layer over said transistor gate region having transistor gate electrical properties, wherein said first dopant has a first conductivity type;

removing said doping barrier;

doping said layer over said transistor gate region and said field oxide region with a second dose of a second dopant so as to form a high resistivity resistor in said layer over said field oxide region ~~without affecting said transistor gate electrical properties~~, wherein said second dopant has a second conductivity type, wherein said first dose of said first dopant is significantly higher than said second dose of said second dopant such that said transistor gate electrical properties are unaffected by said second dose of said second dopant;

forming a silicide blocking oxide layer over an inner portion of said layer over said

field oxide region;

doping an outer portion of said layer over said field oxide region with a third dopant so as to form a high-doped region in said outer portion of said layer over said field oxide region, wherein said third dopant has said second conductivity type;

fabricating a contact region for said high resistivity resistor over said high-doped region in said outer portion of said layer over said field oxide region, wherein said contact region comprises a silicide.

Claim 2 (canceled).

Claim 3 (original): The method of claim 1 wherein said layer comprises polycrystalline silicon.

Claim 4 (previously presented): The method of claim 1 wherein said transistor gate region is a gate of an PFET.

Claim 5 (previously presented): The method of claim 1 wherein said transistor gate region is a gate of an NFET.

Claim 6 (original): The method of claim 1 wherein said field oxide comprises silicon dioxide.

Claim 7 (original): The method of claim 1 wherein said first dopant is an N type dopant.

Claim 8 (original): The method of claim 7 wherein said N type dopant comprises phosphorous.

Claim 9 (previously presented): The method of claim 1 wherein said first dopant comprises phosphorous at a dose of approximately $6.5x10^{15}$ atoms per square centimeter.

Claim 10 (original): The method of claim 1 wherein said second dopant is a P type dopant.

Claim 11 (original): The method of claim 10 wherein said P type dopant comprises boron.

Claim 12 (previously presented): The method of claim 1 wherein said second dopant comprises boron at a dose of approximately $1.0x10^{15}$ atoms per square centimeter.

Claim 13 (canceled).

Claim 14 (currently amended): A method comprising steps of:

depositing a polycrystalline silicon layer on a chip, said polycrystalline silicon layer including a gate region and a resistor region, said gate region being situated over a well and said resistor region not being situated over said well, wherein said field oxide region and said well are situated in a substrate;

forming a doping barrier above said polycrystalline silicon layer so as to prevent doping of said resistor region of said polycrystalline silicon layer;

doping said polycrystalline silicon layer with a first dose of a first dopant, wherein said dose of said first dopant is a dosage greater than required to result in said layer over said gate region having transistor gate electrical properties, wherein said first dopant has a first conductivity type;

removing said doping barrier;

doping said polycrystalline silicon layer with a second dose of a second dopant so as to form a high resistivity resistor in said resistor region of said polycrystalline silicon ~~layer without affecting said transistor gate electrical properties~~, wherein said second dopant has a second conductivity type, wherein said first dose of said first dopant is significantly higher than said second dose of said second dopant such that said transistor gate electrical properties are unaffected by said second dose of said second dopant;

forming a silicide blocking oxide layer over an inner portion of said polycrystalline silicon layer over said field oxide region;

doping an outer portion of said resistor region of said polycrystalline silicon layer

with a third dopant so as to form a high-doped region in said outer portion of said resistor region, wherein said third dopant has said second conductivity type;

fabricating a contact region over said high-doped region in said outer portion of said resistor region of said polycrystalline silicon layer, said contact region being electrically connected to said resistor region, wherein said contact region comprises a silicide.

Claim 15 (original): The method of claim 14 wherein said doping barrier comprises photoresist.

Claim 16 (canceled).

Claim 17 (previously presented): The method of claim 14 wherein said step of doping said polycrystalline silicon layer with a first dopant comprises doping said gate region.

Claim 18 (original): The method of claim 14 wherein said first dopant is an N type dopant.

Claim 19 (original): The method of claim 18 wherein said N type dopant comprises phosphorous.

Claim 20 (previously presented): The method of claim 14 wherein said first dopant comprises phosphorous at a dose of approximately $6.5x10^{15}$ atoms per square centimeter.

Claim 21 (original): The method of claim 14 wherein said second dopant is a P type dopant.

Claim 22 (original): The method of claim 21 wherein said P type dopant comprises boron.

Claim 23 (previously presented): The method of claim 14 wherein said second dopant comprises boron at a dose of approximately $1.0x10^{15}$ atoms per square centimeter.

Claims 24-25 (canceled).